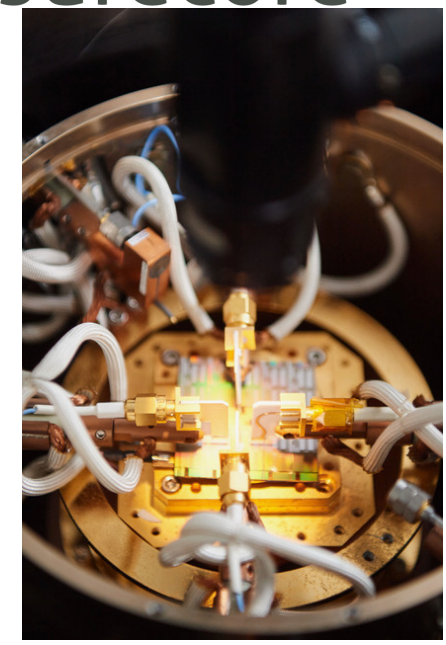
CryoCMOS Consortium develops 4K & 77K transistor models to enable CryoIP development

Sheffield, England – 11 May 2023. The Innovate UK-funded CryoCMOS Consortium, led by sureCore Ltd, reports that it has successfully created new, PDK-quality, transistor models characterised for both 4K & 77K operation. SureCore is using these to develop key foundation IP to enable the design of cryo-control ASICs for use in the quantum computing space. Key to supporting this activity were the accurate cryogenic measurements undertaken by Incize of Louvain-la-Neuve, Belgium.

The challenge posed by Quantum Computing (QC) that this project seeks to address is the effective control of the qubits which will only operate at cryogenic temperatures, typically around 4K, in the confines of a cryostat. The control electronics needed to manipulate the qubits is often located outside the cryostat and can currently only function near to room temperature. This is because silicon chips are only specified to operate from -40°C to 125°C (233K to 398K). Connecting the two requires expensive and bulky cabling, and the amount of cabling required for all the qubits presents a fundamental barrier to QC scaling aside from the inherent latency impact.

If QC is to achieve its potential, then increasing the number of qubits is key. The only solution is to co-locate the control electronics with the qubits in the cryostat. However, given the restricted temperature range of current silicon chips, this is currently not an option. The aim of this project is to understand and model changes in transistor behaviour at cryo temperatures, produce a suite of recharacterized transistor models and then use these to design a portfolio of CryoCMOS IP to facilitate the development of custom chips that can directly interface to the qubits inside the cryostat at cryogenic temperatures.

One of the key transistor parameters affected by plunging temperatures is the threshold voltage (Vt). As the temperature is lowered, the Vt increases substantially, pushing transistor selection towards low and super-low Vt variants (LVt/SLVt). In order to further ease this design challenge, the GLOBALFOUNDRIES 22nm FDSOI (22FDX) process node was selected for this project. FDSOI is an ideal technology choice that allows optimal cryogenic design by enabling adjustments to the threshold voltage to be made by altering the back bias.



Testing inside the cryostat

Key to getting to accurate cryogenic transistor models was the selection of a partner who could make individual transistor measurements. Paul Wells, sureCore's CEO, said, "We picked Incize as it is one of the few commercial companies that specialises in precise cryogenic transistor measurements in the challenging conditions of a cryostat. You can't just rearrange the probes on chip at will in a 4K cryostat. We are really pleased with the quality of the measurement data we received from Incize."

Mostafa Emam, Incize's CEO, commented, "It was a pleasure to work with sureCore and SemiWise on this project to provide our characterization services for cryogenic temperatures. Incize offers a wide range of technology enablement services including characterization and modelling for an extensive range of applications and fabrication process optimisation towards high performance semiconductor devices."

The measurement data was used by SemiWise to develop new transistor models including both Typical-Typical (TT) transistors as well as corners (Slow-Slow, SS & Fast-Fast, FF) that will enable reliable circuit design for use at 4K and 77K. Professor Asen Asenov, SemiWise's CEO, explained, "Standard CMOS is characterised over the usual performance parameters of -40°C to +125°C. So, taking standard CMOS down to 4K or -270°C is a major step into new territory where the operating characteristics of the transistors change markedly." A combination of measurement and simulation data is being used by SemiWise to re-centre the foundry transistor SPICE models for cryogenic temperatures so that the 22FDX node can be used for reliable cryogenic circuit design. The patented SemiWise re-centring technology allows the development of typical and corner transistor models as well as statistical mismatch models, all critical to the SRAM design process. Based on these re-centred cryogenic transistor models, sureCore is exploiting its low power design expertise to develop a suite of power-optimised, foundation IP including Standard Cells, SRAM, ROM and Register Files. Low power is a critical design criterion for the QC space as power consumption translates to unwelcome heating effects which places additional cooling burdens on the cryostat.

Innovate UK awarded a grant of £6.5 million to the CryoCMOS Consortium. This project will help to make cryo-IP available to all UK QC companies so that they will be fast tracked in the race to provide QC solutions and enable the UK to be seen as a centre of excellence for QC. By forming a team of key UK leaders in the field of QC, the project expects

to be able to achieve results in less than three years rather than the many years it would take working as individuals.

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SemiWise
SemiWise develops innovative low-power CMOS transistor-level IP that improves performance and variability, and drastically reduces power consumption. SemiWise also offers simulation services and consulting to the semiconductor industry including fabless, IEDM and foundry players. The CEO of SemiWise, Professor Asenov was the founder of Gold Standard Simulations (GSS), a 2010 start-up from the University of Glasgow which developed the first TCAD based Design-Technology Co Optimisation (DTCO) tool chain. After the acquisition of GSS by Synopsys in 2016, the TCAD-to-Spice technology originally developed by GSS is now part of the Synopsys TCAD offering in the so called TCAD-to-Spice flow and continues to be developed by the Synopsys R&D division in Glasgow:
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