Enabling Cryogenic Chip Design and the Scaling of Quantum Computers

Multiple technologies have been demonstrated for generating and controlling qubits which are in the hearth of every quantum computer (QC). However, QCs have only been realised with a few dozen qubits, whereas to unlock their potential, they need to be scaled to thousands or even millions of qubits.

A QC needs control electronics to manipulate and read out from the qubit array, and to store and process the resulting data. Current implementations typically involve a qubit array chip located in a cryostat, with multiple coaxial cables running to banks of high precision room temperature control electronics. This represents a major barrier to scaling because it's impractical to run thousands of cables into cryostats, and the long cables introduce delays in signal transmission.

In principle, this integration problem can be solved using conventional silicon CMOS fabrication technology bringing the controlling and data processing CMOS chips closer to the qubits in the cryostats. However, existing integrated circuit design methodologies are only validated at temperatures close to room temperature (typically in the range -40oC to +125C), whereas qubit arrays operate at significantly lower temperatures. At such low temperatures commercial process design kits (PDKs) enabling the chip design and verification are not available which currently renders the cryogenic chip design practically impossible. Simultaneously semiconductors exhibit significantly different electronic characteristics at cryogenic temperatures, and the conventional CMOS IP and chip design solutions may not work as intended.

With decades of experience in low-power electronics design and simulation, Semiwise is now creating the necessary IP, know-how and methodology providing the much-needed cryogenic PDKs and enabling the design CMOS circuits optimised for QC applications and operating at cryogenic temperatures but manufactured using conventional foundries. Based on this technology the company will be offering services to recenter the standard foundry process design kits (PDKs) for allowing proper analogue and digital design at cryogenic temperatures. This will minimize the excess heat generated thereby easing the scalability challenges for large quantum computers.

“We are excited to become part of the QC revolution by providing for our customers with the much-needed cryogenic PDKs and enabling cryogenic chip design and IP generation, enabling the QC scaling” commented the CEO of Semiwise, Professor Asenov.

About Semiwise: SemiWise (https://www.semiconductorwise.com/)develops innovative low-power CMOS transistor level IP that improves performance and variability, and drastically reduces power consumption. SemiWise also offers simulation services and consulting to the semiconductor industry including fables, IEDM, and foundry players. The CEO of Semiwise, Professor Asenov was the founder of Gold Standard Simulations (GSS), a 2010 start-up from the University of Glasgow which developed the first TCAD based Design-Technology Co-Optimisation (DTCO) tool chain. After the acquisition of GSS by Synopsys in 2016 the TCAD-to- Spice technology originally developed by GSS is now part of the Synopsys TCAD offering in the so called TCAD-to-Spice (https://www.synopsys.com/silicon/tcad.html/). This technology will be used in the Cryogenic PDK re-centering.

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Note: Professor Asenov is also a Director of Surecore.