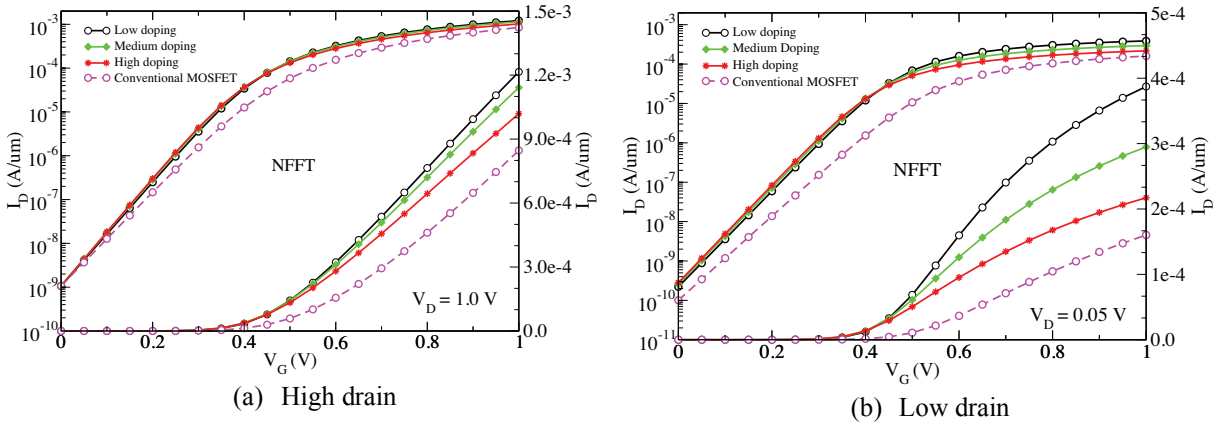
The Flat Field Transistor (FFT) – ideal IoT bulk CMOS technology.

The extremely low power Flat Field Transistor (FFT) technology developed by Semiwise is ideally suited for applications where low power is paramount i.e Internet of Things (IoT) and on chip Artificial intelligence (AI). It is applicable to 40 nm, 28 nm and 20 nm bulk CMOS technologies and scalable to future bulk technology generations.

Semiwise has been working round the clock in order to optimise its Flat Field Transistor (FFT) technology. Here we present the latest results obtained with the most reliable TCAD simulators worldwide: Sentaurus and GARAND. We benchmark a range of FFT transistor designs against standard 20 nm bulk CMOS technology. Figure 1 illustrates the FFT drive current improvement as a function of the doping concentration in the key area of the transistor. The leakage current of the reference and the FFT are aligned at high drain voltage for a fair comparison.



(a) High drain (b) Low drain

Fig. 1 FFT drive current improvement as a function of the doping concentration in the key area of the transistor

Depending on the doping concentration in the technologically important region the FFT can deliver up to 36% performance improvement compared to the reference bulk transistor at high drain bias and more than double the current at low drain bias.

Table 1 low local (purely statistical) variability at V_D= 1.0 V

Doping concentration [cm^{-3}]	σVT_{SAT} [mV]	C2	AV
Low doping	21.7	0.54	0.77
Medium doping	27.3	0.68	0.97
High doping	36.7	0.92	1.29
Conventional MOSFET	64	1.6	2.26

Most importantly the FFT has extremely low local (purely statistical) variability (Table 1) with Av factors in the range of 0.6 mV-µm which is much lower than the reported variability in 14 nm FinFET and 28 nm FDSOI technologies. The extremely low variability of the FFT is ideally suited for near threshold and subthreshold logic and SRAM designs that are emerging necessities for next generation IoT and AI applications.

At all doping concentrations in the technologically important region, the FFT delivers significant performance and variability improvement compared to the reference bulk transistor. This allows seamless control of the threshold voltages without loosing the FFT

benefits. Simultaneously the highest possible benefits can be retained by controlling the threshold voltage using workfunction engineering.

The FFT offers also a better back bias control compared to their bulk counterparts as illustrated in Fig. 2. This is important for achieving very low leakage and power consumption in standby mode.

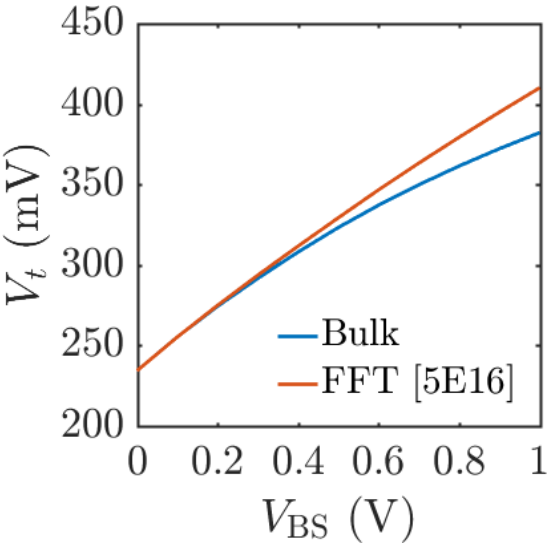


Fig. 2a: Threshold voltage

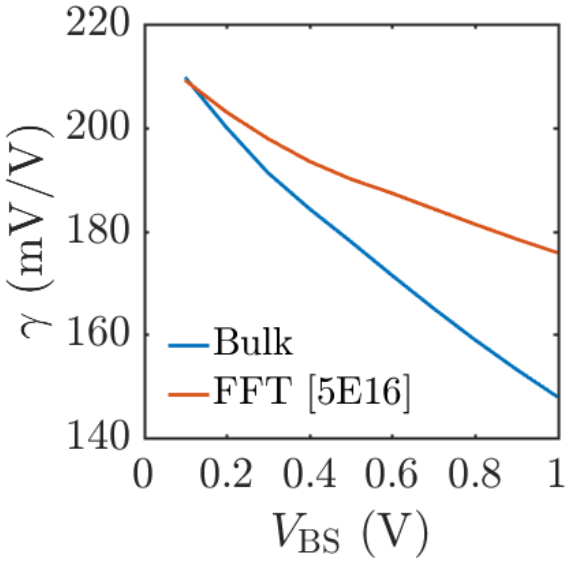


Fig. 2b: Body factor

Fig. 2 Back bias dependence of the threshold voltage and the body factor. V_T is aligned for better comparison.

Fig. 3 (a,b) compared the RTS amplitudes distribution in the FFTs with different doping in the technologically important region and in the reference bulk transistor. The distributions are obtained from a statistical sample of 1000 atomistically different transistors with random position of the RTS trap. It is clear that the RTS amplitudes in the FFT transistor are approximately 3 times lower compared to the reference bulk transistor. This will reduce the jitter and will significantly improve the yield of the corresponding SRAM arrays. Bearing in mind that the Low Noise (LN) power spectrum is directly proportional to ΔI_D^2 distribution and in turn ΔI_D is proportional to ΔV_T the simulations sow that the FFTs will have one order of magnitude lower LF power spectrum compared to the reference bulk transistors.

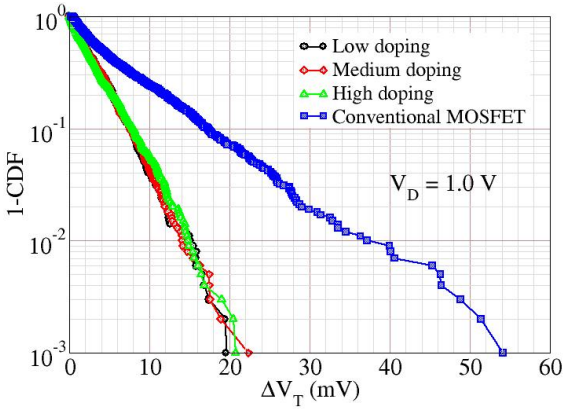


Fig. 3a RTS distribution of 1000 FFT transistors for different doping levels at the V_{DD}=1. 0 V

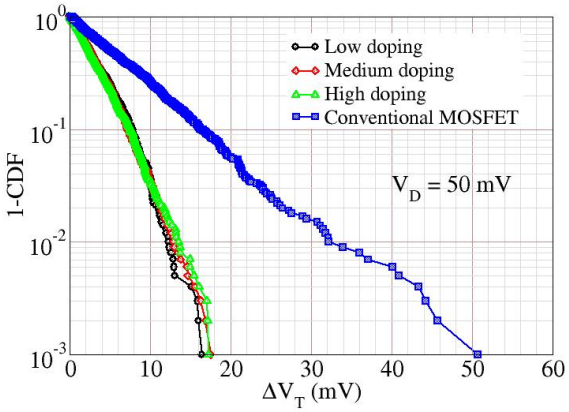


Fig. 3b RTS distribution of 1000 FFT transistors for different doping levels at the V_{DD}=50 mV.

Our analysis shows that the bulk FFT Technology is cheaper than the corresponding bulk CMOS technology counterparts. It also does not require expensive FDSOI substrate.